Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUT 1**
2. **IN 1-**
3. **IN 1+**
4. **VCC**
5. **IN 2+**
6. **IN 2-**
7. **OUT 2**
8. **OUT 4**
9. **IN 4-**
10. **IN 4+**
11. **VCC**
12. **IN 3+**
13. **IN 3-**
14. **OUT 3**

**8**

**7**

**13 12 11 10 9**

**14**

**1**

**2 3 4 5 6**

**DIE ID**

**TL**

**074**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: TL074**

**APPROVED BY: DK DIE SIZE . 082” X .117” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: TL084**

**DG 10.1.2**

#### Rev B, 7/19/02